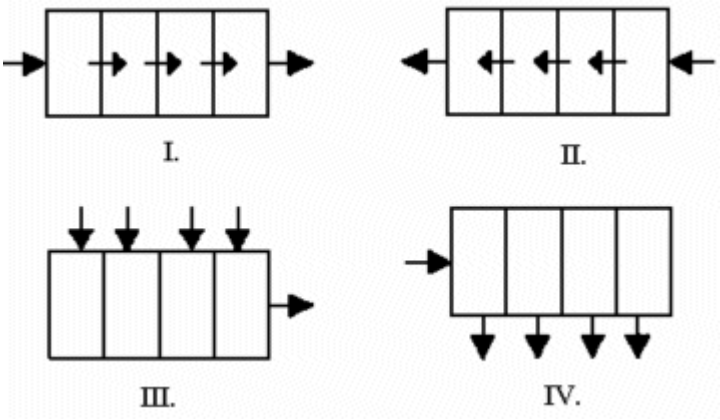
MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

1) The carry output of a half-adder circuit can be expressed as _____.
A) $C_{out} = AB$ B) $C_{out} = A \oplus B$ C) $C_{out} = A + B$ D) None of these

2) What is the major difference between half-adders and full-adders?
A) Half-adders can only handle single digit numbers.
B) Nothing basically; full-adders are made up of two half-adders.
C) Full-adders have a carry input capability.
D) Full-adders can handle double digit numbers.

3) Which of the following is one of the primary functions performed by registers?
A) AND B) XOR C) memory D) NOR

4) Which of the illustrations below represents the parallel-in serial-out register function?



A) Figure I. B) Figure II. C) Figure III. D) Figure IV.

5) How many flip-flops are required to construct a decade counter?
A) 8 B) 4 C) 10 D) 5

6) An active-HIGH input S-R latch has a 1 on the S input and a 0 on the R input. What state is the latch in?
A) $Q = 1, \overline{Q} = 0$ B) $Q = 0, \overline{Q} = 0$ C) $Q = 0, \overline{Q} = 1$ D) $Q = 1, \overline{Q} = 1$

7) What advantage does a J-K flip-flop have over an R-S flip-flop?
A) It has no invalid states. B) It has fewer gates.
C) It has only one output. D) It does not require a clock input.

8) What is one disadvantage of an R-S flip-flop?
A) It has an invalid state. B) It has no Enable input.
C) It has no CLOCK input. D) It has only a single output.

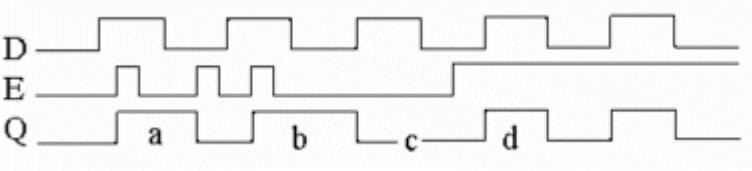
9) Which of the following is correct for a gated D latch?
A) Only one of the inputs can be high at a time.
B) Q output follows the input D when the ENABLE is high.
C) The output complement follows the input when enabled.
D) The output toggles if one of the inputs is held high.

10) Which symbol is used to identify edge-triggered flip-flops?
A) The letter E on the Enable input. B) An inverted "L" on the output.
C) A bubble on the Clock input. D) A triangle on the Clock input.

11) Which of the following describes the operation of a positive edge-triggered D flip-flop?
A) When both inputs are low, an invalid state will exist.
B) The output will follow the input on the leading edge of the clock.
C) The input is toggled into the flip-flop on the leading edge of the clock and is passed to the output on the trailing edge of the clock.
D) If both inputs are high, the output will toggle.

12) If both inputs of an S-R flip-flop are low, what will happen when the clock goes high?
A) The output will toggle.
B) An invalid state will exist.
C) No change will occur in the output.
D) The output will reset.

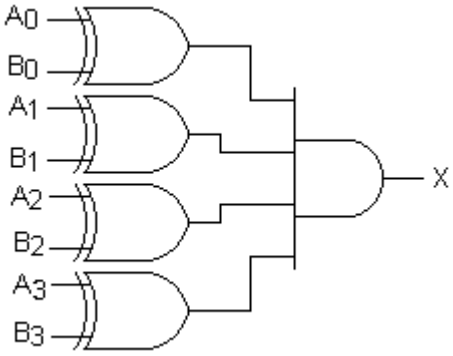
13) These waveforms are applied to a gated D latch, which is initially RESET. Which of the areas identified on the Q waveform is incorrect?



A) Area a
B) Area b
C) Area c
D) Area d

14) Flip-flops are normally used for all of the following applications, except _____.
A) data storage
B) logic gates
C) frequency division
D) counting

15) The circuit below can be used as a(n) _____.



A) 8-bit comparator
B) 4-bit half-adder
C) dual 4-line multiplexer
D) 4-bit comparator

16) The function $A\overline{B}C\overline{D}$ can be decoded with _____.
A) Two 2-input OR gates and two inverters
B) Two 2-input OR gates and one inverter
C) One 4-input AND gate and two inverters
D) One 4-input AND gate and one inverter

17) A BCD-to-decimal decoder has _____ data input lines and _____ data output lines.
A) 7,9
B) 1,10
C) 4, 10
D) 10,10

18) Which of the following is true for IC comparator circuits?
A) All comparators have outputs for indicating A<B, A>B, and A=B.
B) Comparators can compare only 2 bits at a time.
C) Comparators can compare only two values at a time.
D) None of these.

19) A 1-of16 decoder IC has _____ data input connection(s).
A) 1
B) 16
C) 8
D) 4

20) A multiplexer with four select, or address, lines can select one of _____ inputs.
A) 15 B) 7 C) 16 D) 3

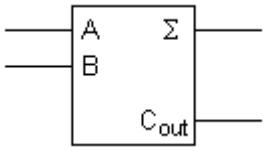


Figure 6–1

21) The symbol in Figure 6–1 represents a(n) _____.
A) Full–adder B) PLD C) AND function D) Half–adder

22) Referring to the symbol in Figure 6–1, which set of outputs is very unlikely to ever occur?
A) $\Sigma = 1, C_{out} = 1$ B) $\Sigma = 1, C_{out} = 0$ C) $\Sigma = 0, C_{out} = 1$ D) $\Sigma = 0, C_{out} = 0$

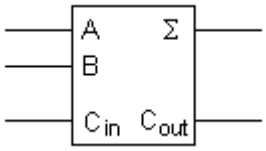


Figure 6–2

23) Refer to the symbol in Figure 6–2. What are the output when A = 1, B = 1, $C_{in} = 0$?
A) $\Sigma = 1,\ C_{out} = 0$ B) $\Sigma = 1,\ C_{out} = 1$ C) $\Sigma = 0,\ C_{out} = 1$ D) $\Sigma = 0,\ C_{out} = 0$

24) The symbol in Figure 6–2 represents a(n) _____.
A) Full–adder B) And function C) Half–adder D) PLD

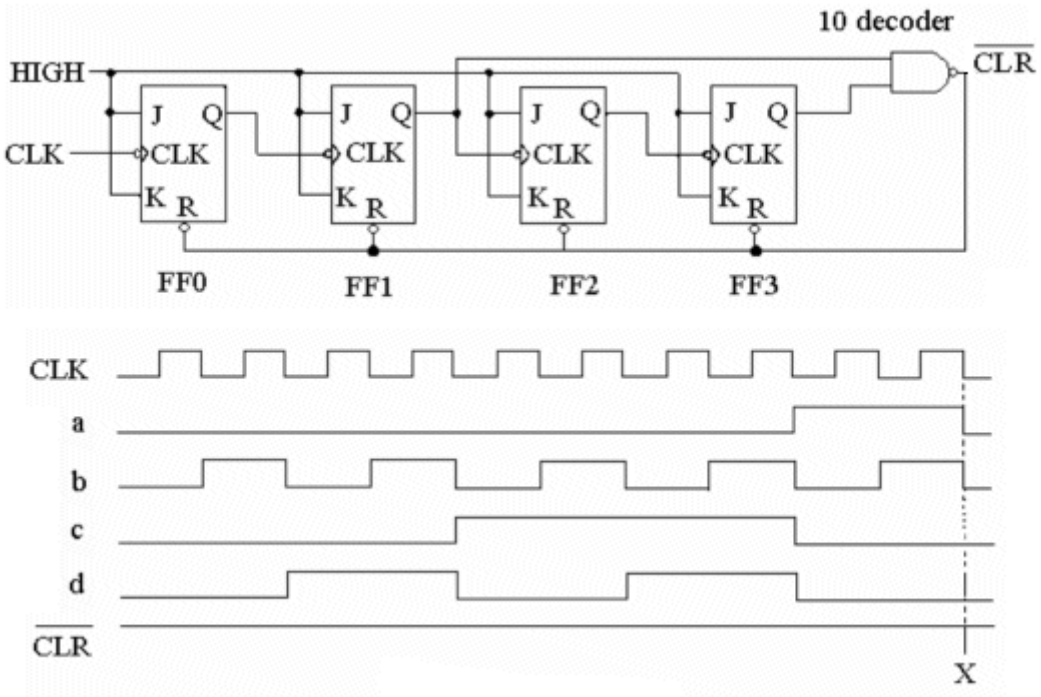


Figure 8–2

25) Which of the waveforms shown in Figure 8– represents the output of FF2?
A) waveform a B) waveform b C) waveform c D) waveform d

26) The circuit in Figure 8–2 is a(n) _____.
A) three–bit synchronous binary counter B) four–bit asynchronous binary counter
C) two–bit asynchronous binary counter D) eight–bit asynchronous binary flip–flop

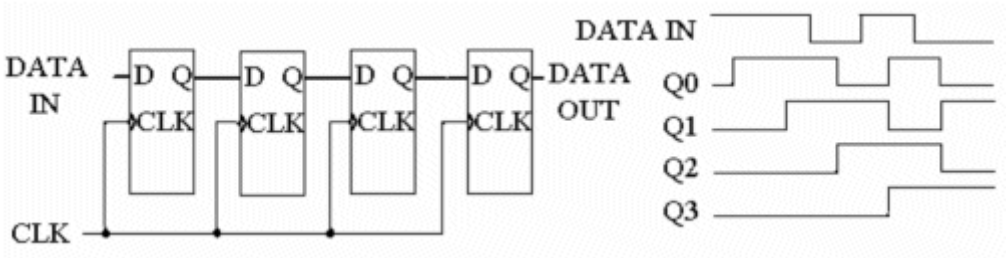


Figure 9–1

27) After the data input shown in Figure 9–1 has been entered into the register, what values are stored in Q3, Q2, Q1, and Q0 respectively?
A) 1 0 0 1 B) 0 1 0 1 C) 1 1 0 1 D) 1 0 1 0

28) How many clock cycles are required to enter the data into the register in Figure 9–1?
A) 32 B) 4 C) 5 D) 31

29) How many data bits can be stored in the register shown in Figure 9–1?
A) 4 B) 32 C) 5 D) 31

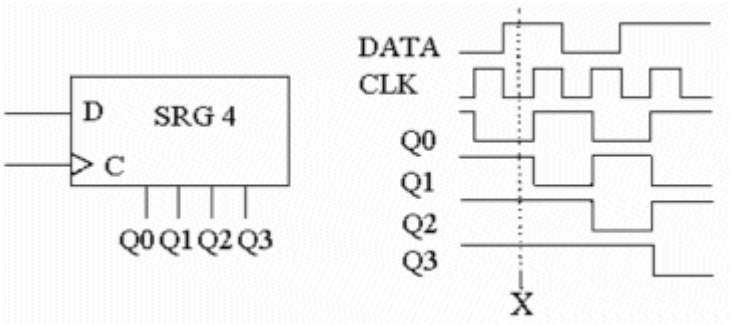


Figure 9–2

30) Refer to the circuit and waveforms in Figure 9–2. What is the value of the data stored in Q3, Q2, Q1 and Q0 respectively at time 'X'?
A) 1 1 1 0 B) 0 1 0 1 C) 0 1 1 0 D) 0 1 1 1

31) Refer to the circuit and waveforms in Figure 9–2. What is the value of the data stored in Q3, Q2, Q1 and Q0 respectively after four clock cycles?
A) 0 1 1 0 B) 1 0 1 0 C) 0 0 0 0 D) 0 1 0 1

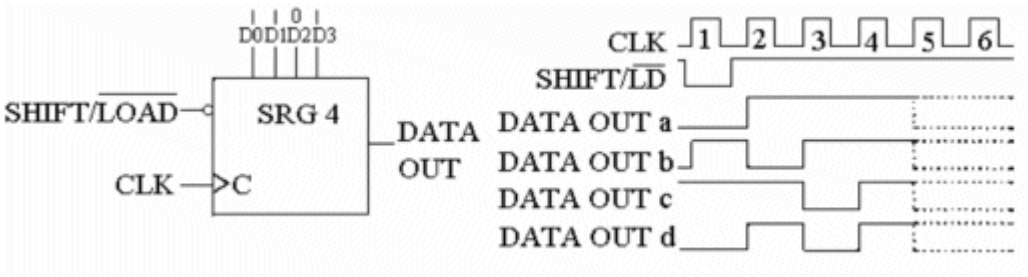


Figure 9–3

32) Which of the DATA OUT waveforms in Figure 9–3 is correct?
A) DATA OUT a. B) DATA OUT b. C) DATA OUT d. D) DATA OUT c.

33) The circuit shown in Figure 9–3 is a _____.
A) serial–in parallel–load register
B) demultiplexer
C) multiplexer
D) parallel–in serial–out register

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

34) Shift registers are used to store and transfer data.

35) A serial–in serial–out shift register transfers data from one line of a parallel bus to another line one bit at a time.

36) A J–K flip–flop can be used as a divide–by–two frequency divider with an output duty cycle of 50%.

37) Parallel–in parallel–out registers have parallel input and output busses.

38) Bidirectional shift registers can shift data either right or left.

39) The term *synchronous* refers to events that do not occur at the same time.

40) Basic counters can be cascaded in parallel to increase the number of data bits that the counter can handle.

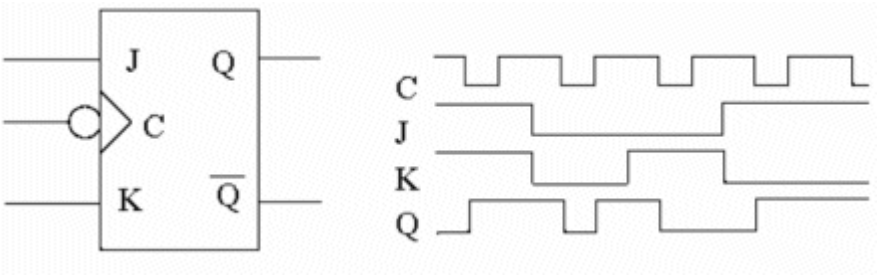
41) The symbol for an edge–triggered flip–flop has a triangle on its clock input.

42) A D flip–flop is constructed by connecting an inverter between the Set and Clock terminals.

43) The J–K flip–flop eliminates the invalid state by toggling when both inputs are high during the transition of the clock signal.

44) In binary addition, 1 + 1 = 10

45) The waveforms for this J–K flip–flop indicate the circuit is operating properly.



46) A group of four bits is called a byte.

47) Full–adders do not provide for a carry input or a carry output.

48) A multiplexer has multiple inputs and a single output.

49) A demultiplexer has multiple inputs and a single output.

50) A half–adder has no carry–in bit.